A 40W Dual-Inductor Hybrid Converter with Flying-Capacitor-Tapped Auxiliary Stage for Fast Transient Response in 48V PoL Automotive Applications

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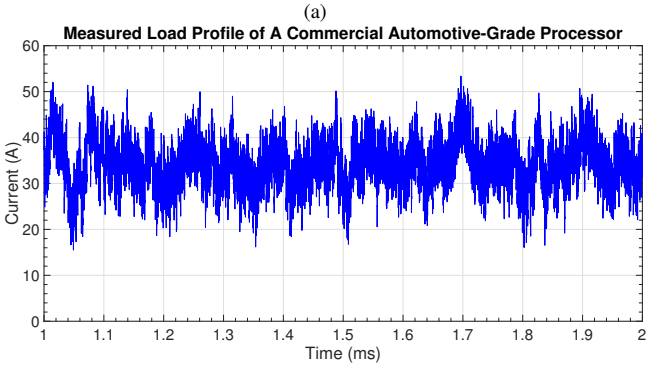
***Abstract*— Advancements in autonomous vehicles have led to a proliferation of onboard electronics, frequently making use of high-performance automotive-grade processors. To satisfy the resulting stringent operating requirements, the dc-dc Power Management Unit (PMU) of the processor must maintain strict voltage regulation, which is typically achieved with large and costly decoupling capacitors. This work proposes an auxiliary-assisted 4-to-1 Dual-Inductor-Hybrid (DIH) converter for fast transient response in 48V-1V applications. The auxiliary converter operates by tapping one of the flying capacitors of the DIH converter and regulates the output voltage using a capacitor-current-based Constant-On-Time control scheme. The 4-to-1 DIH converter acts as the main stage and delivers dc power from the 48V bus by regulating the auxiliary inductor current to avoid drawing dc power through the auxiliary stage. The auxiliary capacitance requirements are relaxed by leveraging the flying capacitor of the DIH converter as an energy reservoir. In simulation, the proposed system operates with a low auxiliary capacitance of 4.7 µF, which creates a 1V deviation on the auxiliary voltage during 20A load transients. A 40W experimental prototype demonstrates the feasibility of the proposed system, achieving a peak efficiency of 93.8%. The prototype regulates the output voltage of 1 V within ±60 mV with an output capacitor of only 650 µF while experiencing load transients up to 12.5 A.**

I. Introduction

With advancements in autonomous vehicles, onboard electronics have come to dominate the cost of automotive systems and currently account for 40% of the total system cost [1]. Consequently, existing 12V distribution networks can no longer supply the power demands of automotive electronics, which reach up to 6 kW [2]. The resulting high transient currents have led to the adoption of 48V networks in automotive systems [3], whose market is expected to increase from 2.22 billion USD in 2019 to 21 billion USD in 2027 [4]. High-performance automotive processors are also becoming more prevalent as the integration of onboard electronics necessitates additional processing power [5], [6]. Various 48V dc-dc Power Management Units (PMUs) have attempted to address the challenge of delivering higher power to processors using advanced hybrid Switched-Capacitor (SC) topologies [7], [8] and custom magnetics [9], [10].

Another challenge for the dc-dc PMUs is the strict regulation of the processor core voltage (typically 0.8 V - 1.2 V) despite the highly variable load profile of the processor and the large 48V-1V conversion ratio. As an example, an autonomous-driving development platform, shown in Fig 1(a), and a measured current profile of its automotive-grade processor is shown in Fig. 1(b). Strict voltage regulation is typically achieved with a high switching frequency in the PMU and large decoupling capacitors, which degrades efficiency and leads to a large PCB footprint, respectively. For the processor shown in Fig. 1(a), a total decoupling capacitance of 5 mF is required to regulate the 1V core voltage with a tolerance of ±3%.

(a)



(b)

Fig. 1: (a) Autonomous-driving development platform with an automotive-grade processor and (b) its measured load profile, with up to 12.5A load transients in 0.4 ms.

The transient response of the PMU can be improved with the use of minimum-deviation control techniques, such

as Constant-On-Time (COT) [11]–[13] and current-mode-control [14]–[16]. Minimum-deviation control schemes adjust the inductor current to the load current within one switching cycle, which minimizes the charge displaced from the output capacitor, C_{OUT}, during load transients. However, the inductor-current slew rate remains constrained by the physical limit imposed by the output LC filter. Thus, further improvements in the transient response of the PMU require alternative power-processing paths.

Low-cost auxiliary converters have been used to improve the transient response of the system. By employing a lower auxiliary inductance, L_{AUX}, than the main stage inductance, the auxiliary stage alleviates the physical limit of the main-stage LC filter on the transient response of the system. To maintain a reasonable current ripple while employing a small L_{AUX}, the auxiliary stage must operate at switching frequencies much higher than the main-stage switching frequency. In [17]–[19], an auxiliary converter is connected in parallel with the main stage to supply current during load transients. Auxiliary converters have typically been presented for 12V distribution networks, but rarely for 48V PoL applications.

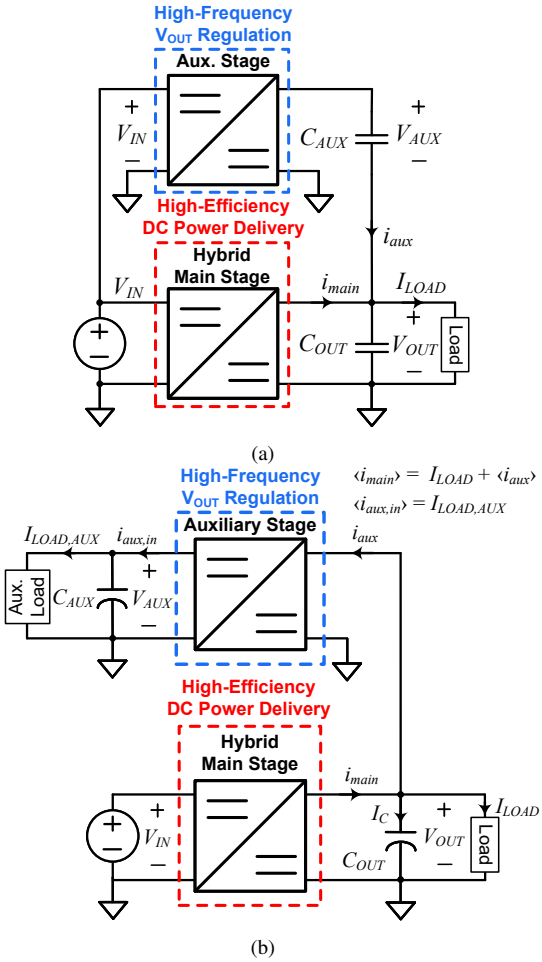


Fig. 2: Existing 48V auxiliary-assisted hybrid converters with (a) adaptive slew rate control, and (b) a V_{IN}-decoupled auxiliary stage.

In [20], an ac-coupled 48V auxiliary stage with adaptive inductor-current slew rate is proposed for output-voltage regulation, as shown in Fig. 2(a). An ac-coupled capacitor is inserted in series with the auxiliary inductor. Adjusting the voltage of this capacitor enables control of the inductor slew rate. However, the auxiliary stage operates directly from the 48V bus, which causes substantial losses due to the high-frequency operation. Due to the voltage derating of capacitors, maintaining the nominal value of the ac-coupled capacitor can be costly as well, when operating with high bias voltages (e.g., $V_{\mathrm{IN}}/2$). In [21], an auxiliary stage regulates the output voltage using a buffer capacitor, C_{AUX}, that is decoupled from the input voltage, V_{IN}, as shown in Fig. 2(b). The 48V main hybrid stage regulates the buffer capacitor voltage, V_{AUX}, to ensure that the input voltage of the auxiliary stage does not collapse. Since the auxiliary stage does not interact directly with the high V_{IN} voltage, it can be optimized for switching losses with the use of low-voltage devices that have better $R_{\mathrm{ON}} \cdot Q_G$ Figure of Merit (FoM). However, a relatively large buffer capacitance is required to ensure that the deviation on V_{AUX} is constrained according to

$$\Delta V_{\mathrm{AUX}} = \int_{t_0}^{t_0+T_{\mathrm{SW,MAIN}}} \frac{\Delta I_{\mathrm{LOAD}} \cdot V_{\mathrm{OUT}}(t)}{C_{\mathrm{AUX}} \cdot V_{\mathrm{AUX}}(t)} dt \qquad (1)$$

where ΔI_{LOAD} is the difference between I_{MAIN} and I_{LOAD}, $T_{\mathrm{SW,MAIN}}$ is the switching period of the main stage, and t_0 is the time at which the load step occurs.

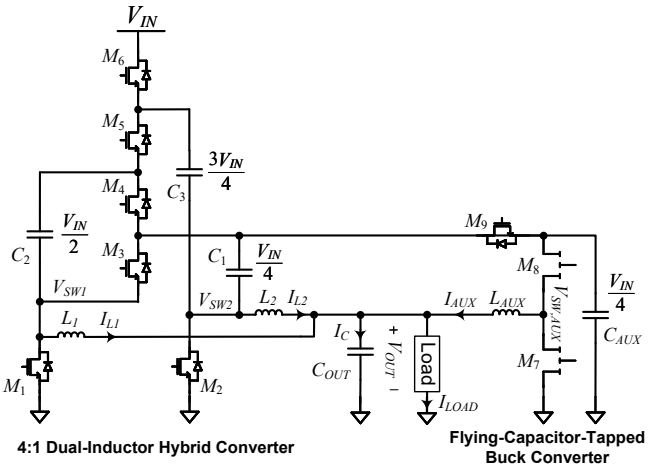


Fig. 3: Proposed hybrid 48V PoL converter with a flying-capacitor-tapped auxiliary stage.

The possibilities for an auxiliary stage are strongly dependent on the choice of the main-stage topology. Hybrid SC converters are becoming popular as the main stage topology in 48V PoL applications due to the large energy density of capacitors. However, the energy stored in the flying capacitors is poorly utilized and is mainly used to step down the input voltage by a factor of N, the native conversion ratio of the hybrid converter. To leverage this underutilized element and address the challenges presented in [20], [21], an auxiliary

converter that operates by tapping the flying capacitor of a 4-to-1 Dual-Inductor Hybrid (DIH) converter as an energy source is presented in this work, as shown in Fig. 3. One of the three flying capacitors acts as an energy reservoir for the auxiliary stage to supply or sink current during load transients to reduce output-capacitance requirements. By tapping the flying capacitor with the lowest voltage, the auxiliary stage also leverages the native conversion ratio of the DIH converter to utilize better-FOM devices for low switching losses.

This paper is organized as follows. The system architecture is presented in Section II, followed by closed-loop simulation results in Section III. Experimental results from the hardware prototype are presented in Section IV, and finally, conclusions are presented in Section V.

II. System Architecture

The proposed architecture, consisting of the DIH main stage and buck auxiliary stage, is shown in Fig. 4. The 4-to-1 Dual-Inductor Hybrid (DIH) converter is selected for the main stage due to its high native conversion ratio and high output-current capability [22]. A balancing controller is typically needed for the flying capacitor voltages of a hybrid switched-capacitor converter to ensure that the device blocking voltages are not exceeded. However, the DIH topology has inherent inductor current and capacitor balancing, which eliminates the need for a current-sharing controller. The flying-capacitor voltages remain balanced whilst still powering the auxiliary stage, so long as the average value of I_{AUX} remains zero. In steady-state operation, the flying capacitor only provides the auxiliary losses, which are quite small and easily replenished by the normal operation of the DIH stage. Although $I_{\mathrm{AUX,ref}}$ can be set to a non-zero value to leverage the auxiliary stage to deliver a portion of the load power, this creates an imbalance in the inductor currents, $I_{\mathrm{L1,2}}$, such that I_{L1} - I_{L2} = I_{AUX}.

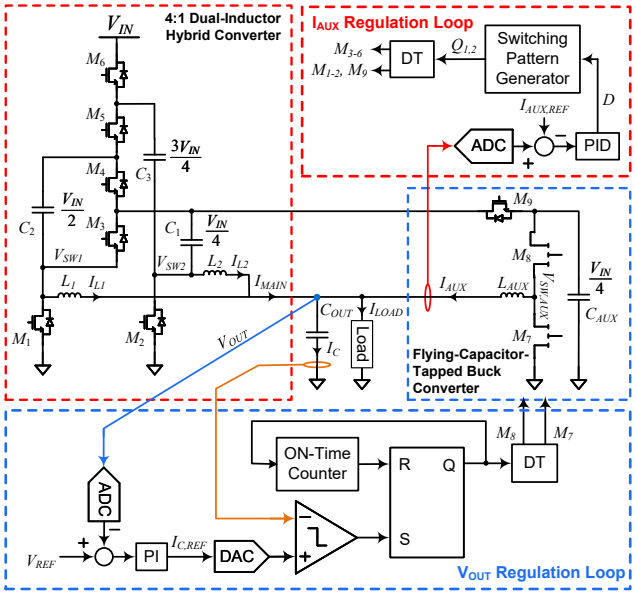


Fig. 4: Control architecture of flying-capacitor-tapped auxiliary stage.

This imbalance can be corrected by compensating the duty cycles of each DIH state, at the expense of unbalancing the flying-capacitor voltages.

The system parameters are presented in Table I. A native DIH conversion ratio of 4 was selected to provide a nominal 12V input voltage for the auxiliary stage, which enables the use of lower-voltage devices with better FoM while still providing sufficient ramp-up capability for I_{AUX}. Since the system has a low output voltage of 1 V, the falling inductor-current slew rate limits the transient performance during step-down load transients. A Constant-On-Time (COT) control scheme based on sensing the output-capacitor current, as shown in Fig. 4, is selected for the auxiliary stage to achieve minimum-deviation response during step-down load transients and maximize the transient performance for a given auxiliary inductance, L_{AUX}. Since L_{AUX} is constrained as it creates an inductive divider with the ESL of the output capacitor, which results in large inductive spikes on V_{OUT}, it is imperative to minimize L_{AUX}. The COT control loop regulates V_{OUT} by adjusting I_{AUX} to ΔI_{LOAD} during transients. By setting $T_{ON,AUX}$ = 60 ns, the auxiliary stage operates at a high switching frequency of almost 1.4 MHz for the nominal auxiliary conversion ratio of 12V-to-1V. By maintaining an auxiliary switching frequency that is 10× higher than $f_{SW,DIH}$, the auxiliary stage can reject most disturbances the main DIH stage imposes on the output node. The DIH main stage in turn regulates I_{AUX} over longer periods using an Average-Current-Mode-Control (ACMC) scheme, shown in Fig. 4, to maintain the average value of I_{AUX} at zero and avoid any steady-state imbalances in $I_{\mathrm{L1,2}}$.

TABLE I: Key System Parameters

Parameter	Value	Unit
Input voltage, V_{IN}	24 - 54	V
Output voltage, V_{OUT}	1	V
Rated Load Power, P_{RATED}	40	W
Max. Load Current Step, ΔI_{LOAD}	20	A
Output Capacitor, C_{OUT}	650	µF
DIH Switching Frequency, $f_{\mathrm{SW,DIH}}$	150	kHz
DIH Native Conversion Ratio, N	4	
DIH Inductors, $L_{1,2}$	1.5	µH
DIH Flying Capacitors, $C_{1,2,3}$	10	µF
AUX On-Time, $T_{\mathrm{ON,AUX}}$	60	ns
AUX Inductor, L_{AUX}	0.12	µH
AUX Capacitor, C_{AUX}	4.7	µF

The switching states of the DIH converter are presented in Fig. 5. Since C_1 is not ground-referenced in State II, the flying capacitor cannot be directly connected to the auxiliary stage. To address this issue, an additional charge-transfer switch, M_9, is used to connect C_1 to the auxiliary stage. By synchronizing M_9 to M_2, the relatively large on-time of the DIH low-side switches, due to the high step-down ratio, enables C_1 to supply the auxiliary losses for the majority of the DIH switching cycle. Nonetheless, the auxiliary capacitance, C_{AUX}, must be sized to ensure that V_{AUX} does not collapse during load transients. When load transients occur, the auxiliary stage responds first such that I_{AUX} = ΔI_{LOAD}, thanks to its fast control loop. While the main-stage control loop adjusts its

operation to bring I_{AUX} back to zero, the auxiliary stage must supply ΔI_{LOAD} for at least $T_{\mathrm{SW,DIH}}$ seconds. The majority of this current is drawn from both C_{AUX} and C_1, which greatly reduces the auxiliary capacitance requirements, as C_1 replenishes C_{AUX} for the majority of the DIH switching cycle.

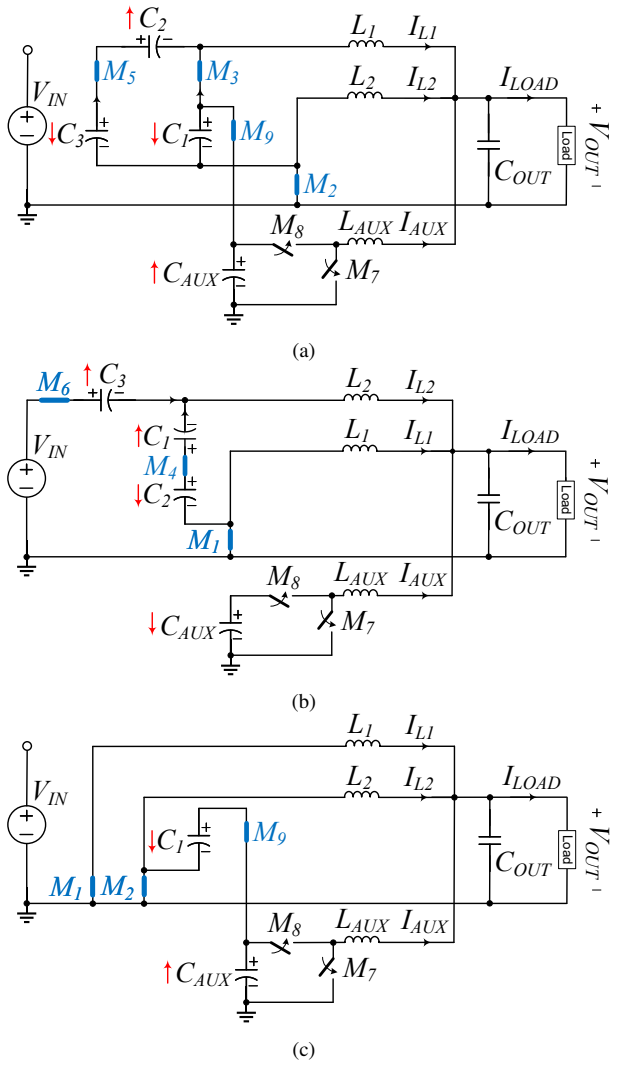


Fig. 5: DIH converter switching states: (a) State I, (b) State II, and (c) State 0.

With the auxiliary stage operating with a COT control scheme, the charge drawn from C_{AUX} in one auxiliary switching cycle can be approximated as

$$Q_{\mathrm{AUX,i}} = \Delta I_{\mathrm{LOAD}} \cdot T_{\mathrm{ON,AUX}} \tag{2}$$

For a given C_{AUX}, the drop in V_{AUX} in one switching cycle can be approximated as

$$\Delta V_{\mathrm{AUX,i}} = \frac{Q_{\mathrm{AUX,i}}}{C_{\mathrm{AUX}} + C_1} \tag{3}$$

Therefore, the total ΔV_{AUX} imposed during a load transient is

$$\Delta V_{\mathrm{AUX}} = \frac{k \cdot \Delta I_{\mathrm{LOAD}} \cdot T_{\mathrm{ON,AUX}}}{C_{\mathrm{AUX}} + C_1}, \tag{4}$$

where k is the ratio of the DIH switching period to the auxiliary switching period and is calculated as follows

$$k = \frac{T_{\mathrm{SW,DIH}} \cdot V_{\mathrm{OUT}}}{T_{\mathrm{ON,AUX}} \cdot \frac{V_{\mathrm{IN}}}{N}}, \tag{5}$$

where $T_{\mathrm{SW,MAIN}}$ is the switching period of the DIH converter. By substituting (5) into (4), the deviation on V_{AUX} for a given C_{AUX} can be determined according to the following equation

$$\Delta V_{\mathrm{AUX}} = \frac{V_{\mathrm{OUT}} \cdot \Delta I_{\mathrm{LOAD}} \cdot T_{\mathrm{SW,DIH}}}{\frac{V_{\mathrm{IN}}}{N} \cdot (C_{\mathrm{AUX}} + C_1)}. \tag{6}$$

Based on the parameters from Table I, the deviation on V_{AUX} is 0.75 V, approximately a 6% deviation from V_{C1}, for ΔI_{LOAD} = 20 A, C_{AUX} = 4.7 µF, C_1 = 10 µF, and a nominal conversion ratio of 48V-to-1V.

III. Simulation Results

The proposed system was validated via a simulation in PLECS, with the parameters shown in Table I. Load steps of 20A were applied to the system to evaluate its transient response. The capacitor-current-based COT control scheme responds to the change in V_{OUT} and rapidly changes I_{AUX} to ΔI_{LOAD}, as shown in Fig. 6. The auxiliary stage continues to provide this current until the change in I_{AUX} is detected by the main DIH stage, which adjusts its inductor currents, $I_{\mathrm{L1,2}}$ until the average value of I_{AUX} returns to zero. Since the auxiliary stage supplies and sinks charge from C_1, its voltage, V_{C1}, deviates from its nominal value of V_{IN}/4 during load transients, as shown in Fig. 7, the impact of which is

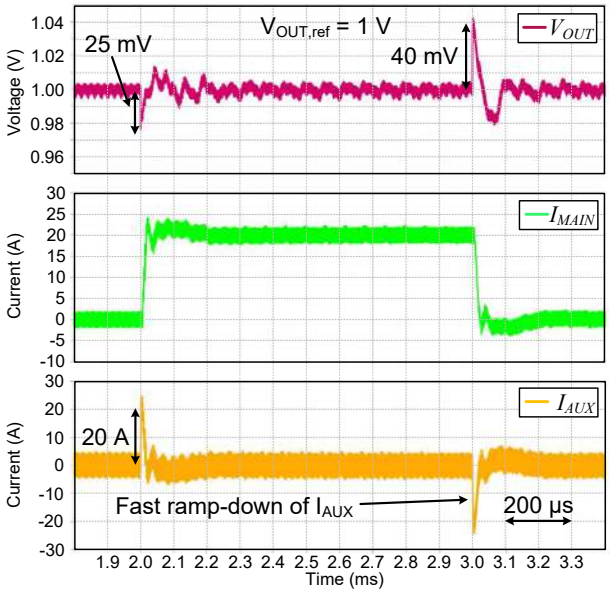


Fig. 6: Simulated output voltage deviation during 20A load steps with V_{IN} = 48 V.

observed in the DIH inductor currents, $I_{L1,2}$. As the lower V_{C1} is applied asymmetrically to each DIH inductor, the DIH inductor currents deviate during transients. However, since the DIH converter has inherent inductor-current and capacitor-voltage balancing, the deviating quantities converge to their nominal values over time.

An output voltage deviation of $40\,\mathrm{mV}$ is observed during the load step-down transient with only $650\,\mu\mathrm{F}$ of output capacitance. With the proposed control scheme, the main stage detects the change in I_{AUX} and adjusts I_{MAIN} to I_{LOAD} within $0.1\,\mathrm{ms}$. Since C_1 provides most of the charge for the auxiliary stage, C_{AUX} is sized relatively small at $4.7\,\mu\mathrm{F}$, which leads to a deviation of $1\,\mathrm{V}$ on V_{C1} as shown in Fig. 7. Due to the high conversion ratio of $48\,\mathrm{V}$-to-$1\,\mathrm{V}$, C_1 is ground-referenced for the majority of the DIH switching cycle, which minimizes the voltage deviation between V_{AUX} and V_{C1}. The DIH inductor currents, $I_{L1,2}$, deviate from their nominal value by up to $7.5\,\mathrm{A}$ due to the variation in V_{C1}, as shown in Fig. 7. Since the DIH converter has inherent inductor-current and capacitor-voltage balancing, this imbalance is automatically corrected to restore uniform current sharing within approximately $1\,\mathrm{ms}$.

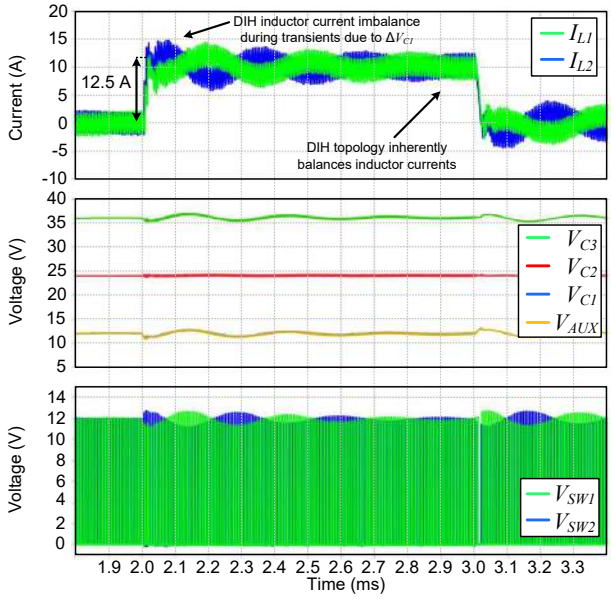


Fig. 7: Simulated DIH inductor current balance due to flying-capacitor voltage deviation during 20A load steps with V_{IN} = 48 V.

To characterize the impact of the auxiliary stage on the transient performance of the system, load transients were applied with the auxiliary stage enabled and disabled, as shown in Fig. 8. When the auxiliary stage is disabled, the main stage directly regulates V_{OUT} using a well-tuned PID controller. For C_{OUT} = $650\,\mu\mathrm{F}$, this results in an overshoot of $330\,\mathrm{mV}$, while the operation of the auxiliary stage limits the overshoot to no more than $40\,\mathrm{mV}$, an $8.25\times$ reduction. As the main-stage inductor current is slew rate limited, its transient performance can be improved only with additional phases.

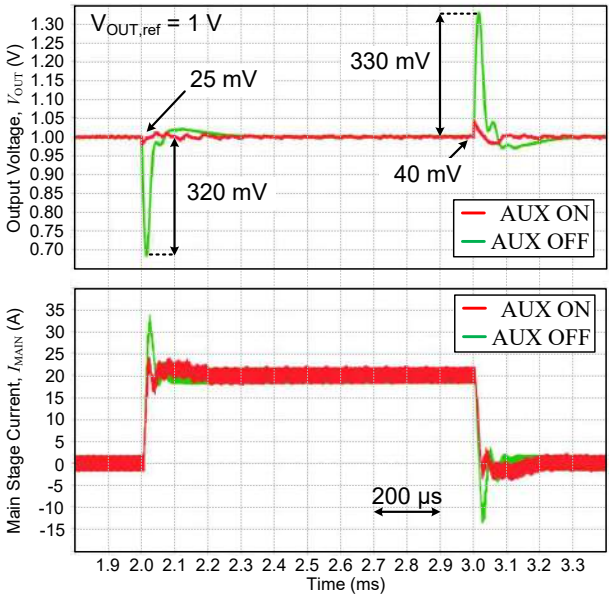


Fig. 8: Simulated load-transient response of the proposed system with the auxiliary stage enabled and disabled.

IV. Experimental Results

To demonstrate the feasibility of the proposed system, a 40W experimental prototype was built, as shown in Fig. 9. To optimize switching losses, 40V GaNFETs were selected for the auxiliary stage and operated at $f_{\mathrm{SW,AUX}}$ = $1.4\,\mathrm{MHz}$. Although it is advantageous for output regulation to maximize $f_{\mathrm{SW,AUX}}$, it is constrained by the low on-time needed for 12V-1V conversion at high frequencies. On the other hand, the DIH switches, M_{1-6}, as well as the charge-transfer switch, M_9, were implemented with low $R_{\mathrm{ds,on}}$ Si MOSFETs to optimize for conduction losses, since they are operated at a much lower frequency.

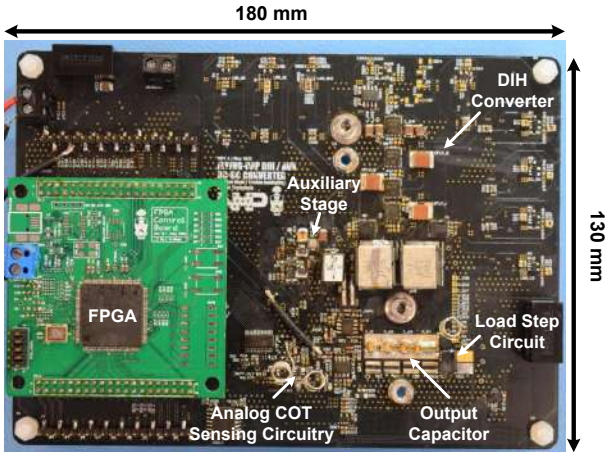


Fig. 9: Experimental prototype of the auxiliary-assisted converter.

The high-speed analog sensing for the capacitor-current-based COT control scheme was implemented on the main power-stage PCB, while the digital ACMC controller was

implemented on the FPGA control board. A high-speed load-transient circuit was also included on the main PCB to generate high-di/dt load steps. The capacitor current was measured using low-ESL current-sensing resistors to ensure that the Power Delivery Network (PDN) was not compromised. To prevent inductive parasitic spikes on V_{AUX}, the charge-transfer switch, M_9 was placed on the backside of the PCB close to C_1, reducing the size of the switching node, while C_{AUX} was placed next to the auxiliary power stage.

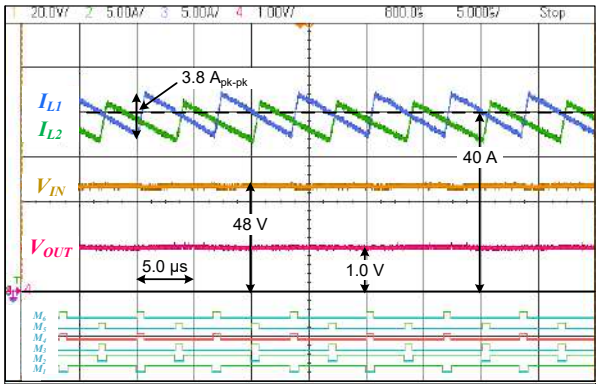


Fig. 10: Measured open-loop steady-state waveforms of the auxiliary-assisted DIH converter.

The open-loop DIH operating waveforms at an output current of 40 A are shown in Fig. 10. The mismatch in the DIH inductor currents of 0.2 A is due to the non-zero I_{AUX}, which was unregulated in this test. A thermal image of the converter at rated load and 48V-1V conversion is shown in Fig. 11. The image highlights that the low-side switches of the DIH converter, $M_{1,2}$, are the main source of losses in the system since they conduct the DIH inductor currents for most of the switching period. A peak temperature of 40.2°C is observed on $M_{1,2}$, indicating relatively low losses.

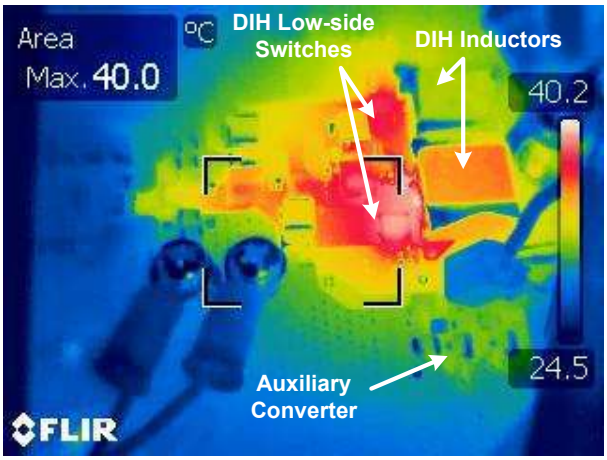
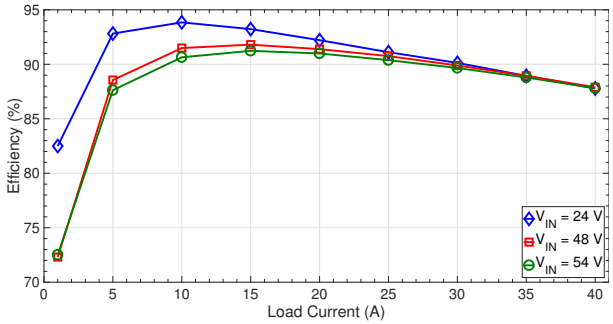


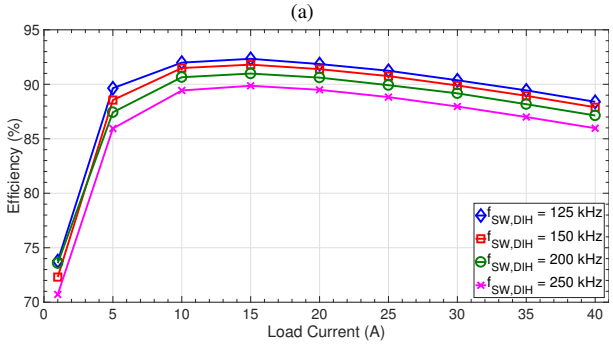
Fig. 11: Thermal image of prototype at I_{LOAD} 40 A and 48V-to-1V direct conversion with forced-air cooling.

The measured system efficiency at V_{OUT} = 1 V for varying V_{IN} is shown in Fig. 12(a). Due to the lower V_{C1} at V_{IN} = 24 V, the auxiliary-stage losses are reduced, which leads to a 4% increase in light-load efficiency at I_{LOAD} = 5 A. A peak efficiency of 93.8% was achieved at I_{LOAD} = 10 A and V_{IN} = 24 V. At the nominal conversion ratio of 48 V-to-1 V, an efficiency of 87.9% was achieved at the rated load of 40 A.

By regulating V_{OUT} with the auxiliary stage, $f_{\mathrm{SW,DIH}}$ is relaxed to reduce the main-stage switching losses, as shown in Fig. 12(b). By reducing $f_{\mathrm{SW,DIH}}$ from 250 kHz to 150 kHz, the efficiency at the rated load is improved by almost 2%. However, a lower $f_{\mathrm{SW,DIH}}$ translates to longer settling times for the I_{AUX} loop. As such, the expected frequency of load transients dictates the minimum limit for the DIH switching frequency.



(a)



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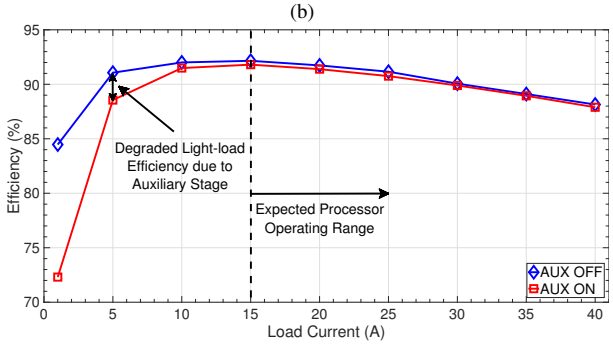

(c)

Fig. 12: Measured system efficiency versus I_{LOAD} at V_{OUT} = 1 V for (a) varying V_{IN}, (b) varying $f_{\mathrm{SW,DIH}}$, and (c) with the auxiliary stage enabled and disabled.

The auxiliary losses significantly impact the light-load efficiency of the converter, as shown in Fig. 12(c). At I_{OUT} = 5 A, a 2.6% drop in efficiency is observed when the auxiliary stage is enabled. However, based on the measurements from

TABLE II: State-of-the-Art 48V Auxiliary-Assisted Converters

	V_{IN} [V]	V_{OUT} [V]	I_{LOAD} [A]	ΔI_{LOAD} [A]	ΔV_{OUT} [mV]	C_{OUT} [µF]	L_{MAIN} [µH]	L_{AUX} [nH]	$m_{F,aux}$ [A/µs]	V_{AUX} [V]	C_{AUX} [µF]
This Work	24-54	1	40	12.5	60	650	1.5	120	8.33	12	4.7
[20]	24-54	1	40	40	40	640	0.47	470	51	12-36	30
[21]	24-70	0.675-0.8	62.5	24	60	720	0.47	36	18.75-22.2	5	120

Fig. 1(b), automotive processors generally operate above 50% rated load power. For this range (20 A - 40 A), the impact of the auxiliary converter on the system efficiency is minimal.

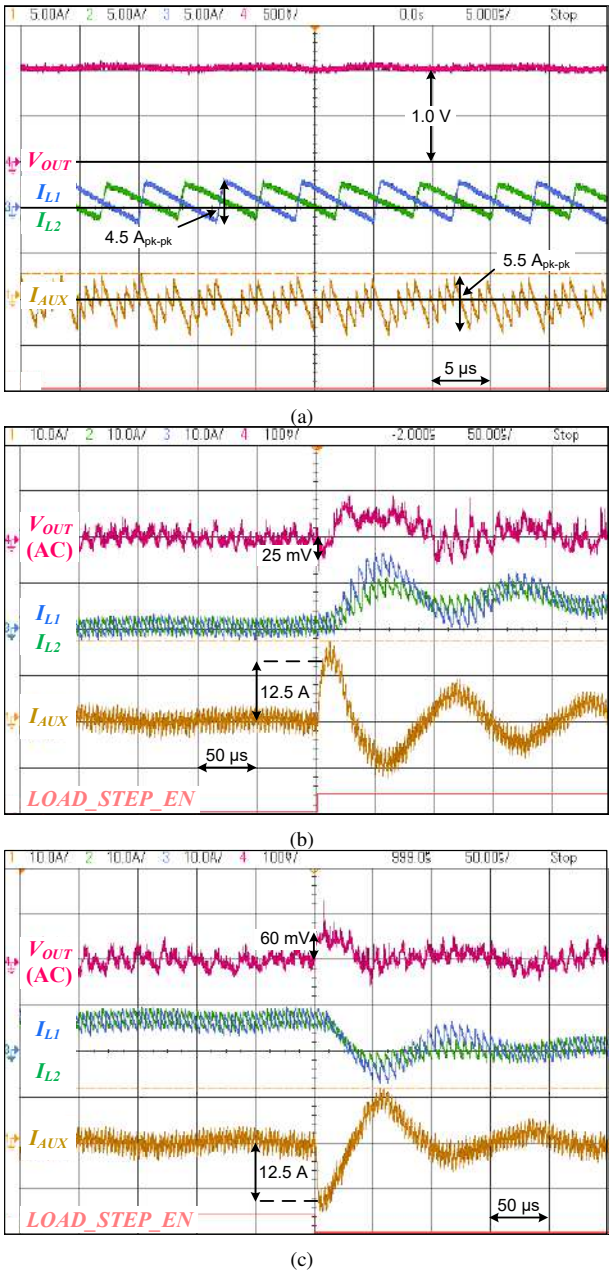

Fig. 13: Measured closed-loop waveforms: (a) steady-state, (b) load step-up, and (c) load step-down transients.

In steady-state closed-loop operation, as shown in Fig. 13(a), the V_{OUT} regulation is performed by the auxiliary stage with I_{AUX} varying at $2 \cdot f_{SW,DIH}$ to reject ΔI_{MAIN}. The DIH inductor currents are well-balanced since I_{AUX} is regulated by the main DIH stage to have zero average value. The prototype regulates the output voltage within $\pm 60\,\text{mV}$ during load steps of $12.5\,\text{A}$ with only $650\,\mu\text{F}$ of decoupling capacitance, as shown in Fig. 13(b) and 13(c). The auxiliary stage must supply the peak transient current from C_1 for a duration of at least $2 \times T_{SW,DIH}$. The deviation in V_{C1} creates an imbalance in $I_{L1,2}$ during load transients that is corrected by the inherent flying-capacitor balancing of the DIH converter.

The performance of the proposed 48V auxiliary-assisted converter is compared to existing 48V auxiliary-assisted converters in Table II. While the proposed system has the lowest inductor-current slew rate, $m_{F,aux}$, it also has the lowest auxiliary capacitance of $4.7\,\mu\text{F}$, which is due to leveraging the flying capacitor of the DIH converter as an energy reservoir for the auxiliary stage.

V. Conclusions

The proposed flying-capacitor-tapped auxiliary converter successfully achieves V_{OUT} regulation with low deviation while significantly reducing the total amount of output capacitance. The auxiliary stage leverages the existing flying capacitor in the main stage as an energy reservoir to supply current during load transients to reduce decoupling-capacitance requirements. The proposed system was simulated with the auxiliary stage enabled and disabled to highlight an $8.25\times$ improvement in voltage overshoot compared to the unassisted main stage. Compared to alternative 48V auxiliary-assisted converters, the auxiliary-capacitance requirements are relaxed. Since the system takes advantage of the short duty cycles of the main stage to effectively use the flying capacitor for buffering the auxiliary input, it can operate with a low auxiliary capacitance of $4.7\,\mu\text{F}$. Load transients of $12.5\,\text{A}$ were applied to the 40W experimental prototype and an output voltage deviation of $\pm 60\,\text{mV}$ was observed with only $650\,\mu\text{F}$ of decoupling capacitance. A peak efficiency of 93.8% was achieved in the 40W experimental prototype, demonstrating the feasibility of utilizing the proposed topology for high-performance automotive power supplies.

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